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EXAMINER	
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ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/965,518	SINDHUSHAYANA ET AL.	
	Examiner	Art Unit	
	Juan A. Torres	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6,7,9-18 and 20-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6,7,9-18 and 20-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 February 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 03/07/2006 has been entered.

Drawings

The modifications to the drawings were received on 03/16/2006. These modifications are accepted by the Examiner.

37 CFR 1.84(p)(4), states "The same part of an invention appearing in more than one view of the drawing must always be designated by the same reference character, and the same reference character must never be used to designate different parts".

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4), because reference character "707", "704", "702", "701", "706", "705", "708" has been used to designate both, "states i-1" and "states i" and "states i+1".

If the intention of the Applicant id to designate the same number for all the different computational nodes C_k (i.e.), then it seems that character "703" in FIG. 7 should be "702". This will be inconsistence with FIG. 6 where properly each states has been labeled with different numbers (see FIG. 6 blocks "604" and "605"; "609" and "610"; "606" and "607"; and "612" and "613")

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The modifications to the specification were received on 03/16/2006. These modifications are accepted by the Examiner.

The disclosure is objected to because of the following informalities: in paragraph [0030], the recitation "The computational nodes associated with the first constituent code 401 at times "i-1," "i" and "i+1" may be respectively represented by a C_{i-1} node 608, a C_i node 609 and a C_{i+1} node 610. The computational nodes associated with the second constituent code 402 at times "k-1," "k" and "k+1" may be represented respectively by a D_{k-1} node 611, a D_k node 612 and a D_{K+1} node 613" is improper; it is suggested to be changed to "The computational nodes associated with the first constituent code 401 at times **"i-1",** "i" and "i+1" may be respectively represented by a C_{i-1} node 608, a C_i node 609 and a C_{i+1} node 610. The computational nodes associated with the second constituent code 402 at times **"k-1",** "k" and "k+1" may be represented

respectively by a D_{k-1} node 611, a D_k node 612 and a $\underline{D_{k+1}}$ node 613" (emphasis added to show the changes).

Appropriate correction is required.

Claim Objections

Claims 6, 7, and 9-13 are objected to because of the following informalities:

As per claim 6, the recitation in line 14 of claim 6 "computational node C at different time instances in said least two subsets occurs concurrently" is improper; it is suggested to be changed to "computational node C at different time instances in said at least two subsets occurs concurrently"

Appropriate correction is required.

As per claims 7 and 9-13, they are objected because they depend directly or indirectly from claim 6.

Response to Arguments

Applicant's arguments filed on 03/16/2006 have been fully considered but they are not persuasive.

Regarding claim 1:

The Applicant contends, "Independent claim 1 has now been amended to recite that the "triggering schedule includes triggering all said computational nodes C and D at different instances of time essentially concurrently for each decoding iteration." Support for this limitation is found in the specification, for example, in numbered paragraph [000481], last four sentences. The admitted prior art does not disclose this limitation.

Applicants respectfully submit that the admitted prior art fails to anticipate independent claim 1 at least for this reason".

The Examiner disagrees, and asserts, that as indicated in the previous Office action, admitted prior art in FIG. 5 shows a method for decoding a sequence of turbo encoded data symbols transmitted over a channel comprising: updating channel nodes R_x, R_y and R_z based on a received channel output (in FIG. 5 R_x is block 501 input 541 and 542; R_y is block 501 input 542 and R_z is block 502 input 540); initializing outgoing messages from symbol nodes X_i, Y_i and Z_k wherein said symbol nodes X_i, Y_i and Z_k are in communication with said channel nodes R_x, R_y and R_z (X_i, is block 501 output 550; Y_i is output of block 520 line 542 and Z_k is output of block 520 line 540); and triggering updates of computational nodes C and D, (computational node C is block 501 and computational node D is block 502) associated with different instances of time, in accordance with a triggering schedule, wherein a computational node C_i is in communication with said symbol nodes X_i, and Y_i and a computational node D_k is in communication with said symbol nodes X_i and Z_k (FIG. 5 input of block 501 – C – have inputs X_i, and Y_i and block 502 – D – have inputs X_i and Z_k); wherein said triggering schedule includes triggering all said computational nodes C and D at different instances of time essentially concurrently for each decoding: iteration (block 501 (computational node C), is the first decoder with inputs, essentially, X (information data) and Y (fist parity), when the first decoder finish, pass the output to block 502 (computational node D), that at a different instant in time, essentially concurrently, with inputs X (information

data) and Z (second parity, or parity from de second encoder) produces the first estimation of the data in iteration zero).

For these reasons and the reason stated en the previous Office Action, the rejection of claim 1 is maintained.

Regarding claim 6:

The Applicant contends, "Claim 6 has been amended and is now in independent form. As amended, the scope of claim 6 is identical or substantially identical to the scope of former claim 8, which has now been canceled. In rejecting claim 8, the Examiner wrote that the admitted prior art of Figure 5 shows "input 541 of block 501 wait until block 502 produces its output 560 and that output is deinterleaved by block 531 and this process is repeated until a determined number of iterations that define a number of subsets that happen a different time instances, each iteration wait for the previous iteration." It appears that this reasoning equates "iteration" with "subset." The concept of a decoding iteration, however, differs from the concept of a subset of computational nodes. An iteration corresponds to a repetition of the triggering schedule, which updates the computational nodes. See, for example, the specification, numbered paragraph [00041], particularly second and third sentences from the end. In contrast, "subsets" refer to computational nodes at different time instances of a symbol sequence. See the "partitioning clause of claim 6., see also the specification, numbered paragraph [00050], particularly the first sentence.

In accordance with the method of claim 6, computational nodes C_0, C_1, C_2, ..., C_N are partitioned into subsets, and nodes in the different subsets are triggered

concurrently for each iteration of decoding. The admitted prior art does not teach such steps. Applicants respectfully submit that the admitted prior art fails to anticipate amended claim 6 (and the now-canceled claim 8) at least for this reason".

The Examiner disagrees, and asserts, that as indicated in the previous Office action, computational nodes C and D, (computational node C is block 501 and computational node D is block 502) associated with different instances of time, in accordance with a triggering schedule, wherein a computational node C_i is in communication with said symbol nodes X_i, and Y_i and a computational node D_k is in communication with said symbol nodes X_i and Z_k (FIG. 5 input of block 501 – C – have inputs X_i, and Y_i and block 502 – D – have inputs X_i and Z_k); wherein said triggering schedule includes triggering all said computational nodes C and D at different instances of time essentially concurrently for each decoding: iteration (block 501 (computational node C), is the first decoder with inputs, essentially, X (information data) and Y (fist parity), when the first decoder finish, pass the output to block 502 (computational node D), that at a different instant in time, essentially concurrently, with inputs X (information data) and Z (second parity, or parity from de second encoder) produces the first estimation of the data in iteration zero. To produce the first iteration (here the term turbo) the information from the decoder 502 have to go to the first decoder 501 as extrinsic information, and the first decoder have to run again producing a new output, for this reason, the computational node C have to have at least two subsets, to produce the first iteration. Without a first iteration the turbo process doesn't take place).

For these reasons and the reason stated en the previous Office Action, the rejection of claim 6 is maintained.

Regarding claims 18 and 22:

The Applicant contends, "Independent claims 18 and 22, as amended, recite concurrent triggering of each node of a first plurality of said computational nodes C, and concurrent triggering of each node of a second plurality of computational nodes D, and should be patentable over the admitted prior art at least for the same reason as claim 6".

The Examiner disagrees, and asserts, that because for the same reason that the rejection of claim 6 is maintained, the rejections of claims 18 and 22 are also maintained

For these reasons and the reason stated en the previous Office Action, the rejection of claims 18 and 22 are maintained.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-3, 6, 7, 9-14, 17, 18 and 20-24 are rejected under 35 U.S.C. 102(a) as being anticipated by admitted prior art in FIG. 5).

As per claim 1, admitted prior art in FIG. 5 shows a method for decoding a sequence of turbo encoded data symbols transmitted over a channel comprising: updating channel nodes R_x, R_y and R_z based on a received channel output (in FIG. 5 R_x

is block 501 input 541 and 542; R_y is block 501 input 542 and R_z is block 502 input 540); initializing outgoing messages from symbol nodes X_i, Y_i and Z_k where the symbol nodes X_i, Y_i and Z_k are in communication with the channel nodes R_x, R_y and R_z (X_i, is block 501 output 550; Y_i is output of block 520 line 542 and Z_k is output of block 520 line 540); and triggering updates of computational nodes C and D, (computational node C is block 501 and computational node D is block 502) associated with different instances of time, in accordance with a triggering schedule, where a computational node C_i is in communication with the symbol nodes X_i, and Y_i and a computational node D_k is in communication with the symbol nodes X_i and Z_k.(FIG. 5 input of block 501 – C – have inputs X_i, and Y_i and block 502 – D – have inputs X_i and Z_k); where the triggering schedule includes triggering all the computational nodes C and D at different instances of time essentially concurrently for each decoding iteration (block 501 (computational node C), is the first decoder with inputs, essentially, X (information data) and Y (fist parity), when the first decoder finish, pass the output to block 502 (computational node D), that at a different instant in time, essentially concurrently, with inputs X (information data) and Z (second parity, or parity from de second encoder) produces the first estimation of the data in iteration zero).

As per claim 2, admitted prior art in FIG. 5 teaches claim 1, admitted prior art in FIG. 5 also teaches decoding a sequence of turbo code where the computational node C_i is in communication with state nodes S_i and S_{i-1}, associated with a first constituent code (FIG. 5 input of block 501 – C – have inputs X_i, with be related to S_i and output X_i will be related with S_{i-1}), and the computational node D_k is in communication with state

node σ_k and σ_{k-1} associated with a second constituent code, where the first and second constituent codes are associated with a turbo code in the communication system used for encoding the sequence of encoded data symbols (FIG. 5 block 501 – C – have inputs X_i, with be related to S_i and output X_i will be related with S_{i-1} and block 502 – D – have inputs X_k, with be related to σ_{k-1} and output X_k will be related with σ_k) .

As per claim 3, admitted prior art in FIG. 5 teaches claim 1, admitted prior art in FIG. 5 also teaches accepting a value of symbol X_i at the symbol node X_i as a decoded value of symbol X_i after at least one iteration of the triggering updates of the computational nodes C and D (FIG. 5 output of block 501 line 550 after the first cycle).

As per claim 6, admitted prior art in FIG. 5 shows a method for decoding a sequence of turbo encoded data symbols transmitted over a channel comprising: updating channel nodes R_x, R_y and R_z based on a received channel output (in FIG. 5 R_x is block 501 input 541 and 542; R_y is block 501 input 542 and R_z is block 502 input 540); initializing outgoing messages from symbol nodes X_i, Y_i and Z_k where the symbol nodes X_i, Y_i and Z_k are in communication with the channel nodes R_x, R_y and R_z (X_i, is block 501 output 550; Y_i is output of block 520 line 542 and Z_k is output of block 520 line 540); and triggering updates of computational nodes C and D, (computational node C is block 501 and computational node D is block 502) associated with different instances of time, in accordance with a triggering schedule, where a computational node C_i is in communication with the symbol nodes X_i, and Y_i and a computational node D_k is in communication with the symbol nodes X_i and Z_k.(FIG. 5 input of block 501 – C – have inputs X_i, and Y_i and block 502 – D – have inputs X_i and Z_k); partitioning the

computational node C at time instances C_0, C_1, C_2, ... , C_N into at least two subsets, where the triggering schedule includes triggering updates of computational nodes C in a sequence at different time instances in each subset (FIG. 5 input 541 of block 501 wait until block 502 produces its output 560 and that output is deinterleaved by block 531 and this process is repeated until a determined number of iterations that define a number of subsets) and where the triggering of computational node C at different instances in the at least two subsets occurs concurrently (block 501 (computational node C), is the first decoder with inputs, essentially, X (information data) and Y (fist parity), when the first decoder finish, pass the output to block 502 (computational node D), that at a different instant in time, essentially concurrently, with inputs X (information data) and Z (second parity, or parity from de second encoder) produces the first estimation of the data in iteration zero. To produce the first iteration (here the term turbo) the information from the decoder 502 have to go to the first decoder 501 as extrinsic information, and the first decoder have to run again producing a new output, for this reason, the computational node C have to have at least two subsets, to produce the first iteration. Without a first iteration the turbo process doesn't take place).

As per claim 7, admitted prior art in FIG. 5 teaches claim 6, admitted prior art in FIG. 5 also teaches determining the sequence at different time instances in each subset for the triggering updates FIG. 5 input 541 of block 501 wait until block 502 produces its output 560 and that output is deinterleaved by block 531 and this process is repeated until a determined number of iterations that define a number of subsets that happen a different time instances, each iteration wait for the previous iteration).

As per claim 9, admitted prior art in FIG. 5 teaches claim 1, admitted prior art in FIG. 5 also teaches that the at least two subsets of computational node C at different time instances C_0, C_1, C_2, ... , C_N have at least one common computational node time instance FIG. 5 input 541 of block 501 wait until block 502 produces its output 560 and that output is deinterleaved by block 531 and this process is repeated until a determined number of iterations that define a number of subsets that happen a different time instances, each iteration wait for the previous iteration. The block 501 will hold the value Y_i of waiting for the next value of X_i, X_{i+1} that will be in a common computational node time instance).

As per claim 10, admitted prior art in FIG. 5 teaches claim 6, admitted prior art in FIG. 5 also teaches partitioning computational node D at different time instances D_0, D_1, D_2, ... , D_N into at least two subsets, where the triggering schedule includes triggering computational nodes D at different time instances in a sequence in each subset (FIG. 5 input 532 of block 502 wait until block 501 produces its output 550 and that output is interleaved by block 530 and this process is repeated until a determined number of iterations that define a number of subsets).

As per claim 11, admitted prior art in FIG. 5 teaches claim 10, admitted prior art in FIG. 5 also teaches determining the sequence at different time instances in each subset for the triggering updates (FIG. 5 input 532 of block 502 wait until block 501 produces its output 550 and that output is interleaved by block 530 and this process is repeated until a determined number of iterations that define a number of subsets that happen a different time instances, each iteration wait for the previous iteration).

As per claim 12, admitted prior art in FIG. 5 teaches claim 10, admitted prior art in FIG. 5 also teaches that the triggering of computational node D at different time instance in the least two subsets occurs concurrently (FIG. 5 input 532 of block 502 wait until block 501 produces its output 550 and that output is interleaved by block 530 and this process is repeated until a determined number of iterations that define a number of subsets that happen a different time instances, each iteration wait for the previous iteration. The block 502 will hold the value Z_k of waiting for the next value of X_k, X_{k+1}).

As per claim 13, admitted prior art in FIG. 5 teaches claim 10, admitted prior art in FIG. 5 also teaches that the subsets of computational node D at time instances D_0, D_1, D_2, ... , D_N have at least one common computational node time instance (FIG. 5 input 532 of block 502 wait until block 501 produces its output 550 and that output is interleaved by block 530 and this process is repeated until a determined number of iterations that define a number of subsets that happen a different time instances, each iteration wait for the previous iteration. The block 502 will hold the value Z_k of waiting for the next value of X_k, X_{k+1} that will be in a common computational node time instance).

As per claim 14, admitted prior art in FIG. 5 teaches claim 1, admitted prior art in FIG. 5 also teaches that the updating includes summing incoming messages to produce an output message, and outputting the output message for updating (FIG. 5 input 541 of block 501 X_i 2^{nd} estimation will produce an updated output in 550 that will be the third estimation).

As per claim 17, admitted prior art in FIG. 5 teaches claim 1, admitted prior art in FIG. 5 also teaches that the sequence of data includes "N" number of symbols, each

symbol in the sequence is identified by either a subscript "i" or "k," and the subscript "i" and "k" are references to time instances in the decoding process (FIG. 5 subscript "i" is input to block 501 related with not-interleaved data and subscript "k" is input to block 502 related with interleaved data).

As per claim 18, admitted prior art in FIG. 5 shows a method for decoding a sequence of turbo encoded data symbols transmitted over a channel comprising: updating channel nodes R_x, R_y and R_z based on a received channel output (in FIG. 5 R_x is block 501 input 541 and 542; R_y is block 501 input 542 and R_z is block 502 input 540); initializing outgoing messages from symbol nodes X_i, Y_i and Z_k where the symbol nodes X_i, Y_i and Z_k are in communication with the channel nodes R_x, R_y and R_z (X_i, is block 501 output 550; Y_i is output of block 520 line 542 and Z_k is output of block 520 line 540); state nodes S_i and S_{i-1} associated with a first constituent code in a turbo code (in FIG. 5 block 501 output 550 and inputs 541 and 542); state nodes σ_k and σ_{k-1} associated with a second constituent code in the turbo code (in FIG. 5 block 502 output 560 and inputs 540 and 532); a computational node C_i in communication with the symbol nodes X_i and Y_i (computational node C_i is block 501); and a computational node D_k in communication with the symbol nodes X_i and Z_k (computational node D_k is block 502), where the computational node C_i is in communication with the state nodes S_i and S_{i-1} (in FIG. 5 block 501 output 550 and inputs 541 and 542) and the computational node D_k is in communication with the state nodes σ_k and σ_{k-1} (in FIG. 5 block 502 output 560 and inputs 540 and 532); a computational node C_{i+1} in communication with the state node S_i (in FIG. 5 block 501 inputs 541 and 542); a computational node C_{i-1}, in

communication with the state node S_{i-1} (in FIG. 5 block 501 output 550); a computational node D_{k+1} in communication with the state node σ_k (in FIG. 5 block 502 inputs 540 and 532); and a computational node D_{k-1} in communication with the state node σ_{k+1} (in FIG. 5 block 502 output 560), where computational nodes C and D at different time instances are configured for updates in accordance with a update triggering schedule and the update triggering schedule including concurrent triggering of each node of a first plurality of the computational nodes C, and concurrent trickery of each node of a second plurality of computational nodes D (block 501 (computational node C), is the first decoder with inputs, essentially, X (information data) and Y (fist parity), when the first decoder finish, pass the output to block 502 (computational node D), that at a different instant in time, essentially concurrently, with inputs X (information data) and Z (second parity, or parity from de second encoder) produces the first estimation of the data in iteration zero. To produce the first iteration (here the term turbo) the information from the decoder 502 have to go to the first decoder 501 as extrinsic information, and the first decoder have to run again producing a new output, for this reason, the computational node C have to have at least two subsets, to produce the first iteration. Without a first iteration the turbo process doesn't take place).

As per claim 20, admitted prior art in FIG. 5 teaches claim 18, admitted prior art in FIG. 5 also teaches that the update triggering schedule includes triggering updates in a sequence in a partitioned computational nodes C_0, C_1, C_2, ... , C_N of at least two subsets and in a sequence in a partitioned computational nodes D_0, D_1, D_2, ... , D_N of at least two subsets (FIG. 5 input 541 of block 501 wait until block 502 produces its output

560 and that output is deinterleaved by block 531 and this process is repeated until a determined number of iterations that define a number of subsets, input 532 of block 502 wait until block 501 produces its output 550 and that output is interleaved by block 530 and this process is repeated until a determined number of iterations that define a number of subsets).

As per claim 21, admitted prior art in FIG. 5 teaches claim 18, admitted prior art in FIG. 5 also teaches that the sequence of data includes "N" number of symbols, where each symbol in the sequence is identified by either a subscript "i" or "k" corresponding to the subscripts used for the state nodes and the computational nodes (FIG. 5 subscript “i” is input to block 501 related with not-interleaved data and subscript “k” is input to block 502 related with interleaved data).

As per claim 22, admitted prior art in FIG. 5 shows a processor configured for decoding a sequence of turbo encoded data symbols for communication over a channel comprising: channel nodes R_x, R_y and R_z for receiving channel output (in FIG. 5 R_x is block 501 input 541 and 542; R_y is block 501 input 542 and R_z is block 502 input 540); symbol nodes X_i, Y_i and Z_k in communication with the channel nodes R_x, R_y and R_z (X_i, is block 501 output 550; Y_i is output of block 520 line 542 and Z_k is output of block 520 line 540); state nodes S_i and S_{i-1} associated with a first constituent code in a turbo code (in FIG. 5 block 501 output 550 and inputs 541 and 542); state nodes σ_k and σ_{k-1} associated with a second constituent code in the turbo code (in FIG. 5 block 502 output 560 and inputs 540 and 532); a computational node C_i in communication with the symbol nodes X_i and Y_i (computational node C_i is block 501); and a computational node

D_k in communication with the symbol nodes X_k and Y_k (computational node D_k is block 502), where the computational node C_i is in communication with the state nodes S_i and S_{i-1} (in FIG. 5 block 501 output 550 and inputs 541 and 542) and the computational node D_k is in communication with the state nodes σ_k and σ_{k-1} (in FIG. 5 block 502 output 560 and inputs 540 and 532); a computational node C_{i+1} in communication with the state node S_i (in FIG. 5 block 501 inputs 541 and 542); a computational node C_{i-1} in communication with the state node S_{i-1} (in FIG. 5 block 501 inputs 541 and 542); a computational node D_{k+1}in communication with the state node σ_k (in FIG. 5 block 502 inputs 540 and 532); and a computational node D_{k-1} in communication with the state node σ_{k+1} (in FIG. 5 block 502 output 560), where computational nodes C and D at different time instances are configured for updates in accordance with a update triggering schedule and the update triggering schedule including concurrent triggering of each node of a first plurality of the computational nodes C, and concurrent trickery of each node of a second plurality of computational nodes D (block 501 (computational node C), is the first decoder with inputs, essentially, X (information data) and Y (fist parity), when the first decoder finish, pass the output to block 502 (computational node D), that at a different instant in time, essentially concurrently, with inputs X (information data) and Z (second parity, or parity from de second encoder) produces the first estimation of the data in iteration zero. To produce the first iteration (here the term turbo) the information from the decoder 502 have to go to the first decoder 501 as extrinsic information, and the first decoder have to run again producing a new output, for

this reason, the computational node C have to have at least two subsets, to produce the first iteration. Without a first iteration the turbo process doesn't take place).

As per claim 23, admitted prior art in FIG. 5 teaches claim 22, admitted prior art in FIG. 5 also teaches that the update triggering schedule includes triggering updates of the computational nodes C and D in a sequence of C_0, C_1, C_2, . . . , C_N, C_{N-1}, C_{N-2}, C_{N-3}, . . . C_2, C_1, C_0, D_0, D_1, D_2, . . . , D_N, D_{N-1}, D_{N-2}, D_{N-3}, . . . D_2, D_1, D_0 (FIG. 5 input 532 of block 502 wait until block 501 produces its output 550 and that output is interleaved by block 530 and this process is repeated until a determined number of iterations).

As per claim 24, admitted prior art in FIG. 5 teaches claim 22, admitted prior art in FIG. 5 also teaches that the sequence of data includes "N" number of symbols, where each symbol in the sequence is identified by either a subscript "i" or "k" corresponding to the subscripts used for the state nodes and the computational nodes (FIG. 5 subscript "i" is input to block 501 related with not-interleaved data and subscript "k" is input to block 502 related with interleaved data).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 15 and 16 rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art as applied to claim 1 above, and further in view of Xu (US 20010052104).

As per claim 15, admitted prior art discloses claim 1. Admitted prior art in FIG. 5 discloses a method for decoding a sequence of turbo code where the updating of the channel nodes R_x, R_y and R_z based on the received channel output includes receiving at the channel node R_x the channel output associated with a symbol X_i; receiving at the channel node R_y the channel output associated with a symbol Y_i; receiving at the channel node R_z the channel output associated with a symbol Y_k; passing from the channel node R_x a next value of the symbol X_i, based on the received channel output, to the symbol node X_i; passing from the channel node R_y a next value of the symbol Y_i, based on the received channel output, to the symbol node Y_i; and passing from the channel node R_z a next value of the symbol Z_k, based on the received channel output, to the symbol node Z_k. FIG. 5 doesn't teach that the next value is a representation of the likelihood of the value, but this is inhering in the process of turbo decoding, a new update in a value will represent the likelihood of this value in comparison with the previous value, this is very well known in turbo decoding process and Xu teaches the process of passing from the channel node R_x a likelihood of the symbol X_i, based on the received channel output, to the symbol node X_i; passing from the channel node R_y a likelihood of the symbol Y_i, based on the received channel output, to the symbol node Y_i; and passing from the channel node R_z a likelihood of the symbol Z_k, based on the received channel output, to the symbol node Z_k (Figure 3 page 2 paragraph [0018]). Teaches of FIG. 5 and Xu teachings are analogous art because they are from the same field of endeavor. Even it is inherit in FIG. 5 at the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the likelihood of the

value as disclosed by Xu with the turbo decoder disclosed in FIG. 5. The suggestion/motivation for doing so would have been to determine when to stop the iteration process.

As per claim 16, admitted prior art in FIG. 5 shows a method for decoding a sequence of turbo code where the initializing outgoing messages from symbol nodes X_i, Y_i and Z_k includes: passing a message from the symbol node X_i to the computational node C_i of the computational node C, where the message is based on a summation of incoming messages at the symbol node X_i (FIG. 5 input 541 of block 501 with previous values input 542 of block 501); passing a message from the symbol node X_i to the computational node D_k of the computational node D, where the message is based on a summation of incoming messages at the symbol node X_i (FIG. 5 input 532 of block 502 with previous values input 540 of block 502); passing a message from the symbol node Y_i to the computational node C_i (FIG. 5 input 542 of block 501); and passing a message from the symbol node Z_k to the computational node D_k (FIG. 5 input 540 of block 502). It is inherit that passing a message from the symbol node Y_i to the computational node C_i is based in the likelihood of the data symbol (input 541 of block 501). It is inherit that passing a message from the symbol node Z_k to the computational node D_k is based in the likelihood of the data symbol (input 532 of block 502). This is very well known in turbo decoding process and Xu teaches that passing a message from the symbol node Y_i to the computational node C_i is based in the likelihood of the data symbol (Figure 3 L_a page 2 paragraph [0018]). It is inherit that passing a message from the symbol node Z_k to the computational node D_k is based in the likelihood of the data symbol (Figure 3 L_{e1}

page 2 paragraph [0018]). Teaches of FIG. 5 and Xu teachings are analogous art because they are from the same field of endeavor. Even it is inherit in FIG. 5 at the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the likelihood of the value as disclosed by Xu with the turbo decoder disclosed in FIG. 5. The suggestion/motivation for doing so would have been to determine when to stop the iteration process.

Conclusion

All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is (571) 272-3119. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Juan Alberto Torres
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